Please amend the claims to read as follows:

Listing of Claims

1. (Currently Amended) An interleaving/deinterleaving method for interleaving/deinterleaving first data stored in data storage means to second data so that ~~the~~ an arrangement of ~~the~~ data elements of said second data is different from ~~the~~ an arrangement of ~~the~~ data elements of said first data, comprising:

a first step of reading word data, part of said first data, from said data storage means, and

a second step of selecting a data element to be processed from said word data read and of outputting said selected data element, said first step and said second step being repeated, wherein

~~the~~ a sequence of said data elements to be processed at the time of the repetition is determined in accordance with the arrangement of the data elements of said second data.

2. (Currently Amended) An interleaving/deinterleaving method for interleaving/deinterleaving first data stored in data storage means to second data so that ~~the~~ an arrangement of ~~the~~ data elements of said second data is different from ~~the~~ an

4

arrangement of ~~the~~ data elements of said first data in bit units, comprising:

a first step of reading word data, part of said first data, from said data storage means, and

a second step of selecting a data element to be processed from said word data read and of outputting said selected data element,

a third step of shifting a bit sequence having already been stored in a shift register by one bit and of storing said data element selected and output in said shift register, and

a fourth step of storing the bit sequence stored in said shift register in said data storage means after the processing from said first step to said third step is repeated by a predetermined number of times, wherein

~~the~~ a sequence of said data elements to be processed at the time of the repetition of the processing from said first step to said third step is determined in accordance with the arrangement of the data elements of said second data.

3.   (Currently Amended) An interleaving/deinterleaving method for interleaving/deinterleaving first data stored in data storage means to second data so that ~~the~~ an arrangement of ~~the~~

data elements of said second data is different from ~~the~~ <u>an</u>

arrangement of ~~the~~ data elements of said first data, comprising:

a step of initializing an area, in which said second data is

stored, of said data storage means,

a step of reading word data, part of said first data, from

said data storage means in accordance with the arrangement of the

data elements of said first data and of storing said word data in

a shift register,

a step of sequentially shifting out said word data stored in

said shift register beginning with the data element positioned in

the most significant bit position,

a step of generating first word data by positioning said

data element shifted out at a bit position in word data serving

as said second data and by expanding said data element to word

data,

a step of reading as second word data the word data stored

at the address of said data storage means in which said data

element shifted out should be stored,

a step of computing ~~the~~ <u>a logic</u> OR of said first word data

with said second word data, and

a step of storing ~~said~~ <u>the logical</u> OR <u>result</u> at the address,

from which said second word data is read, in said data storage

means.

6

4. (Currently Amended) An interleaving/deinterleaving apparatus for interleaving/deinterleaving first data stored in data storage means to second data so that ~~the~~ an arrangement of ~~the~~ data elements of said second data is different from ~~the~~ an arrangement of ~~the~~ data elements of said first data, comprising:

data storage means for storing said first data,

access information supply means for sequentially supplying the address information of word data, part of said first data, in said data storage means and the bit position information of ~~the~~ a data element to be processed in said word data, and

data selection means for receiving the word data read from the address, corresponding to said address information, of said data storage means, for selecting one data element from said word data on the basis of said bit position information and for outputting said data element, wherein

said address information and said bit position information supplied sequentially by said access information supply means are determined in accordance with the arrangement of the data elements of said second data.

5. (Original) An interleaving/deinterleaving apparatus in accordance with claim 4, wherein

said data elements are processed in bit units,

7

a shift register for sequentially shifting, by one bit, a bit sequence having already been stored and for sequentially storing a 1-bit data element sequentially output from said data selection means is further provided, and

when the bit width of said bit sequence stored in said shift register reaches a predetermined bit width, not smaller than the bit width of at least 1-word data, said bit sequence is stored as part of said second data in said data storage means.

6. (Original) An interleaving/deinterleaving apparatus in accordance with claim 4, wherein said data selection means comprises a shifter, said word data read from said data storage means is shifted so that the data element to be selected is positioned at a specific bit position, and the output from said specific bit position after the shifting is used as the output of said data selection means.

7. (Currently Amended) An interleaving/deinterleaving apparatus for interleaving/deinterleaving first data stored in data storage means to second data so that ~~the~~ an arrangement of ~~the~~ data elements of said second data is different from ~~the~~ an arrangement of ~~the~~ data elements of said first data, comprising:

8

data storage means for storing said first data and said
second data,

access information supply means for supplying the address
information of word data, part of said second data, in said data
storage means and the bit position information of ~~the~~ a data
element to be processed in said word data,

a shift register for storing word data, part of said first
data, read from said data storage means in accordance with the
arrangement of the data elements of said first data and for
sequentially shifting out said word data beginning with the data
element positioned in the most significant bit position,

data expansion means for sequentially expanding said data
element shifted out sequentially from said shift register on the
basis of said bit position information to word data and for
outputting said word data, and

logical OR means for computing ~~the~~ a logical OR of said word
data read from the address, corresponding to said address
information, of said data storage means with said word data
output from said data expansion means and for outputting ~~said~~ the
logical OR result, wherein

said logical OR result output from said logical OR means is
stored at the address, corresponding to said address information,

from which said word data is read, of said data storage means, and

said address information and said bit position information supplied sequentially by said access information supply means are determined in accordance with the arrangement of the data elements of said first data.

8. (Original) An interleaving/deinterleaving apparatus in accordance with claim 7, wherein said data expansion means comprises a shifter, said data element shifted out from said shift register is shifted so as to be positioned in the bit position corresponding to said bit position information, 0 is set in the bits higher and lower than the bit position corresponding to said bit position information, and the obtained data is output as word data.

Claims 9-12   (Cancelled).

13. (New) An interleaving/deinterleaving apparatus for interleaving/deinterleaving first data stored in data storage means to second data so that an arrangement of data elements of said second data is different from an arrangement of data elements of said first data, the apparatus comprising:

10

data storage means for storing said first data and said second data;

access information supply means for supplying address information and bit position information;

a shift register for storing word data, part of said first data, read from said data storage means in accordance with the arrangement of the data elements of said first data and for sequentially shifting out said word data beginning with the data element positioned in the most significant bit position at the time of interleaving;

data selection expansion means for sequentially expanding said data element shifted out sequentially from said shift register on the basis of said bit position information to word data and for outputting said word data at the time of interleaving; and

logical OR means for computing a logical OR of word data read from the address, corresponding to said address information, of said data storage means with said word data output from said data selection expansion means and for outputting the logical OR result at the time of interleaving, wherein:

said address information designates an address of word data, part of said second data, in said data storage means at the time of interleaving or designates an address of word data, part of

said first data, in said data storage means at the time of deinterleaving,

said bit position information designates the bit position of a data element to be processed in said word data, part of said second data, at the time of interleaving or designates the bit position of a data element to be processed in said word data, part of said first data, at the time of deinterleaving,

said logical OR result output from said logical OR means is stored at the address, corresponding to said address information, from which said word data is read, of said data storage means,

said data selection expansion means receives said word data read from the address, corresponding to said address information, of said data expansion means, selects one data element from said word data on the basis of said bit position information and outputs said data element at the time of deinterleaving, and

said shift register sequentially shifts, by one bit, a bit sequence having already been stored and sequentially stores a 1-bit data element sequentially output from said data selection expansion means at the time of deinterleaving, and when the bit width of said bit sequence stored in said shift register reaches a predetermined bit width, not smaller than the bit width of at least 1-word data, said bit sequence is stored as part of said second data in said data storage means.

12

14. (New) An interleaving/deinterleaving apparatus for interleaving/deinterleaving first data stored in data storage means to second data so that an arrangement of data elements of said second data is different from an arrangement of data elements of said first data, the apparatus comprising:

data storage means for storing said first data and said second data;

access information supply means for supplying address information and bit position information;

a shift register for storing word data, part of said first data, read from said data storage means in accordance with the arrangement of the data elements of said first data and for sequentially shifting out said word data beginning with the data element positioned in the most significant bit position at the time of deinterleaving;

data selection expansion means for sequentially expanding said data element shifted out sequentially from said shift register on the basis of said bit position information to word data and for outputting said word data at the time of deinterleaving; and

logical OR means for computing a logical OR of said word data read from the address, corresponding to said address information, of said data storage means with said word data

13

output from said data selection expansion means and for

outputting the logical OR result at the time of deinterleaving,

wherein:

said address information designates an address of word data,

part of said second data, in said data storage means at the time

of deinterleaving or designates an address of word data, part of

said first data, in said data storage means at the time of

interleaving,

said bit position information designates the bit position of

a data element to be processed in said word data, part of said

second data, at the time of deinterleaving or designates the bit

position of a data element to be processed in said word data,

part of said first data, at the time of interleaving,

said logical OR result output from said logical OR means is

stored at the address, corresponding to said address information,

from which said word data is read, of said data storage means,

said data selection expansion means receives said word data

read from the address, corresponding to said address information,

of said data expansion means, selects one data element from said

word data on the basis of said bit position information and

outputs said data element at the time of interleaving, and

said shift register sequentially shifts, by one bit, a bit

sequence having already been stored and sequentially stores a

14

1-bit data element sequentially output from said data selection

expansion means at the time of interleaving, and when the bit

width of said bit sequence stored in said shift register reaches

a predetermined bit width, not smaller than the bit width of at

least 1-word data, said bit sequence is stored as part of said

second data in said data storage means.